AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 14, line 18, as follows:

Figure 1 is a block diagram illustrating a data processing system in which the synchronisation techniques of preferred embodiments of the present invention may be employed. As shown in Figure 1, a processor core 40 is coupled to an instruction cache or other memory device 10 from which instructions required by the processor core 40 may be accessed. Within the processor core 40, a prefetch unit 20 is provided for issuing over path 50 requests for instructions determined by the prefetch unit to be required by the pipelined processor 30. The instruction memory 10 from which the instructions are retrieved then outputs the instructions back to the prefetch unit 20 over path 60, from where they are then passed over path 70 into the pipelined processor 30. When executing instructions, the pipelined processor 30 will interface with registers of register bank 35 containing data values to be manipulated by the instructions. ~~Load~~ Via paths 85 and 90, load instructions may be used to load data values into the register bank from the data memory 87, and store instructions may be used to store data values into the data memory 87 from the register bank 35. Data processing instructions may then be executed on the data values stored in particular registers of the register bank 35.

Please amend the paragraph beginning at page 29, line 1, as follows:

The decoder 205 decodes the instruction written into buffer A 900 as soon as it arrives and the subsequent buffers, B 910 and C 920, receive the decoded version of the instruction in buffer A. The A flag 930 now indicates that the data in A are valid and also represent a coprocessor instruction. Thus non-coprocessor or unrecognized instructions are immediately dropped from the instruction queue and are never passed on. The coprocessor also compares the coprocessor number field in a coprocessor instruction and compares it with its own. If the

number doesn't match, the instruction is invalid. The buffer flags 940 and 950 and the multiplexers 960, 970 operate in the same manner as described earlier with reference to the buffer flags 640, 650 and multiplexers 660, 670 of Figure 6.